MATLAB EXPO 2019

Top Down Modeling and Analysis of Analog Mixed-Signal Systems

Rajesh R. Berigei
Worldwide Semiconductor Manager, MathWorks
Agenda

- What is Top Down Modeling and Analysis
- Why is Top Down relevant to Analog Mixed-Signal (referred to as AMS)
- Tools, Flows and Methodology to support a Top Down AMS workflow
- Using a Top Down AMS Workflow to implement
  - Phased Locked Loop
  - Analog to Digital Converter
  - SerDes (was covered in previous talk)
What is Bottoms-up Analysis

Assemble AMS building blocks and analyze via simulation
AMS building blocks: MOS, BJT, Diodes, Resistors, Capacitor, Logic Gates

MATLAB EXPO 2019
Charge Pump
Simulation Time: Seconds to Minutes

Video Cable Equalizer
Simulation Time: Hours to Days
Other Pitfalls Of Bottoms-up Analysis

- Limited Design Abstractions
- Design Trade-offs hard to analyze
- Low Verification Confidence
- Specification Isolated From Verification
- Disconnected Tools
- Slow Design Iterations
- Disconnected Teams

Complexity

Quality

Efficiency and Reuse
What is Top Down Modeling and Analysis

Integrating a pulse train

System Model

Behavioral Netlist

Schematics Netlist

MATLAB EXPO 2019
To Tapeout
“In a top-down approach, the architecture of the chip is defined as a block diagram and simulated and optimized using a system simulator such as Matlab or Simulink. From the high-level simulation, requirements for the individual circuit blocks are derived.”
Usage of Tools in a Top Down AMS Framework

**Mixed-Signal Blockset**
- Explore various architectures
- Model impairments
- Fast tradeoff analysis to select best architecture to meet specifications

**Simulink**
- Validate architecture in Simulink
- Export Behavioral model to Virtuoso
- High level testbench cosimulation management with AMS Designer

**Virtuoso**
- Start with initial behavioral model netlist from Simulink
- Implement schematics for each block
- Co-simulate each schematic block with high level system model in Simulink

**Tapeout**
- DRC
- LVS
- Other tapeout checks
PLL Design
Architectural Selection With Mixed-Signal Blockset

- Measurement testbenches
- Phase noise analysis
- White-box architectural models
- Building blocks with impairments
- Open and closed-loop analysis
Explore Various PLL Architectural Models

Model PLL and ADCs using architectural models
- Integer-N PLLs
- Fractional-N PLLs
- Flash, SAR ADCs
PLL Model Refinement – Impairments

- Get started in your design using building blocks including impairments:
  - Finite rise and fall time
  - Leakage, imbalance
  - Phase noise
  - Aperture jitter
  - PLL lock time and frequency
  - PLL phase noise profile
Configure Each PLL Component and Run

- Model AMS behavior and impairments using your specs
- Perform open and closed-loop PLL analysis
Validate Selected Architecture in Simulink
Export PLL Behavioral Model to AMS Designer

1. C Code
2. SystemVerilog (DPIC) wrapper
3. Incisive / AMS Designer

Challenges
Replace PLL Charge Pump With Detailed Virtuoso Schematics
Co-simulate Simulink With AMS Designer

Two variable step solvers working together
Charge-pump being simulated in Spectre
Rest of the PLL system simulated in Simulink
Similar Methodology and Tool Flow can be Applied to ADC
Summarizing Top-Down AMS Tool Flow Methodology

**Simulink**
- Explore AMS Architecture in MS Blockset or SerDes Toolbox
- Validate Behavioral Model in Simulink
- Export Behavioral Model to Cadence
- Implement AMS design in Cadence
- Co-simulate Simulink with Spectre
- Post process simulation data to optimize model

**SystemVerilog Export**

**Cadence**

**SerDes Toolbox**

**Mixed-Signal Blockset**

**Simulink-Spectre Co-simulation**
Mixed-Signal Blockset – Batteries Included!

**PLL**
- PLL Tutorial
- PLL Behavioral Model with Impairments
- Voltage Controlled Oscillator including Phase Noise
- PLL 2.4GHz including Cadence Virtuoso AMS Designer Analog Cosimulation
- PLL 50x including different Measurements
- PLL with Dual Modulus Prescaler
- Fractional N PLL

**ADC**
- ADC Tutorial including Cadence Incisive Digital Cosimulation
- ADC Behavioral Model with Impairments and Measurements
- Interleaved ADC
- Subranging ADC
- Successive Approximation ADC
- 3rd Order Sigma-Delta ADC including Circuit Level Implementation
- 4th Order Sigma-Delta ADC

**Equalization**
- SerDes Tutorial
- Backplane Modeling Workflow and App
- 64b/66b Coding
- 64b/67b Coding
- 8b/10b Coding
- Tunable Equalizer and Bathtub Curve Generation with Statistical Approach and Parallel Simulation
- Clock Recovery
- SerDes 10 Gbps
- SerDes 2 Gbps with Circuit-Level CTLE

**SMPS**
- Switched Mode Power Supply Tutorial
- Boost
- Buck
- Flyback
- SEPIC

www.mathworks.com/campaigns/products/offer/mixed-signal.html
Other Resources on AMS at MathWorks

- **Self Paced Learning**
  - [MATLAB and Simulink for Mixed-Signal Systems](#)
  - [Simulink Onramp](#)
  - [MATLAB Onramp](#)

- **Available on Request**
  - Hands-on Analog Mixed-Signal Workshop
  - Hands-on SerDes Workshop
  - Seminar, presentation and demo of Analog Mixed-Signal workflows