MATLAB EXPO 2016 KOREA

4월 28일 (목)

등록 하기 matlabexpo.co.kr



Product Code Generation and Real-Time Testing

김종헌 차장 Senior Application Engineer MathWorks Korea





Agenda

Production Code Generation

- MathWorks' Code Generation Products
- Embedded Coder
- Equivalence Test with SIL and PIL
- Integration Test
 - What's Simulink Real-Time
 - Automation of Real-Time Testing



Code Generation Products

MATLAB Coder

Generate C and C++ code from MATLAB code

Simulink Coder

Generate C and C++ code from Simulink and Stateflow models

Embedded Coder

Generate C and C++ code optimized for embedded systems



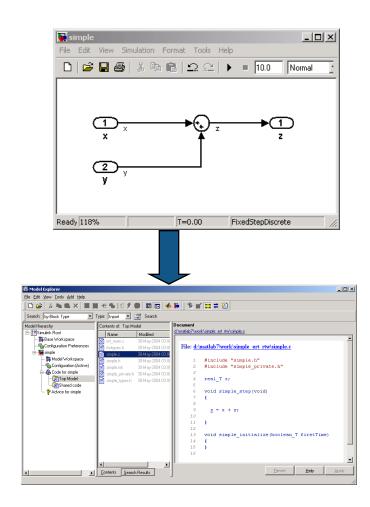
Code Generation Products: Simulink Coder and Embedded Coder

Simulink Coder

- Generates code for use in simulation and prototyping applications
- Comes with Generic Real-Time (GRT) based targets

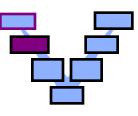
Embedded Coder

- Generates efficient code that can be customized to look like hand code for production
- Comes with Embedded Real-Time (ERT) based targets

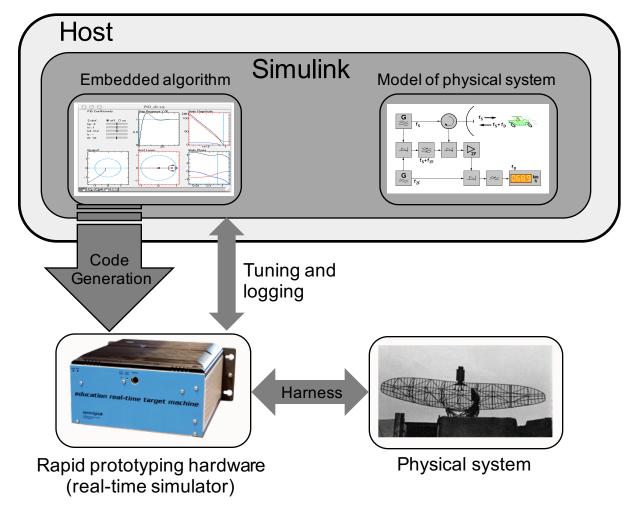




Rapid Prototyping Simulink Coder with Simulink Real-Time



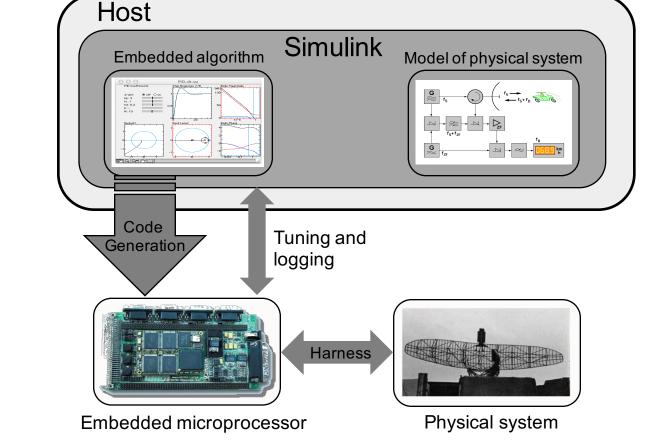
Generate, deploy, and tune code for a component (algorithm or controller) on a real-time simulator connected to system hardware

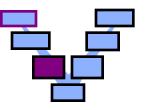


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Rapid Prototyping on Embedded Processors Embedded Coder

Run the generated code in real time, tune parameters, and monitor real-time data on the same processor you plan to use in mass production, or a close equivalent to it.

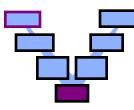








Production Code Generation Embedded Coder



Select Target

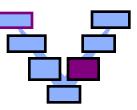
öystem Target File:	Description:
asap2.tlc	ASAM-ASAP2 Data Definition Target
autosar.tlc	AUTOSAR
ert.tlc	Embedded Coder
ert.tlc	Create Visual C/C++ Solution File for
ert_shrlib.tlc	Embedded Coder (host-based shared lik
grt.tlc	Generic Real-Time Target
grt.tlc	Create Visual C/C++ Solution File for
grt_malloc.tlc	Generic Real-Time Target with dynamic
grt_malloc.tlc	Create Visual C/C++ Solution File for
idelink_ert.tlc	IDE Link ERT
idelink_grt.tlc	IDE Link GRT
realtime.tlc	Real-Time Toolbox
rsim.tlc	Rapid Simulation Target
rtwin.tlc	Real-Time Windows Target
rtwinert.tlc	Real-Time Windows Target (ERT)
rtwsfcn.tlc	S-Function Target
tlmgenerator.tlc	SystemC TLM Component Generator
tornado.tlc	Tornado (VxWorks) Real-Time Target
xpctarget.tlc	xPC Target
xpctargetert.tlc	xPC Target (ERT)
•	4
ull Name: C:\MATLAB	\R2012b\rtw\c\ert\ert.tlc
emplate Makefile: ert_default_	_tmf
/lake Command: make_rtw	
_	

Choose Optimizations and File Packaging

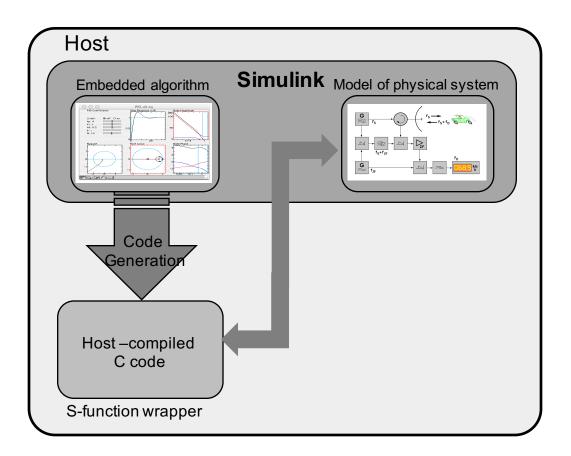
Software environment					
Code replacement library:	C89/C90 (ANSI)				
Shared code placement:	C89/C90 (ANSI) C99 (ISO)				
Support: 📝 floating-point n	GNU99 (GNU) AUTOSAR 4.0				
📝 absolute time	TI C28x (ISO)				
📃 variable-size si	TI C28x TI C55x (ISO)				
Multiword type definitions:	TI C55x TI C62x (ISO)				
Code interface	TI C62x TI C64x				
🔲 Classic call interface	TI C64x+ TI C67x				
🔲 Generate reusable code	TI C672x TI C674x				
Generate preprocessor con					
🔲 Suppress error status in	real-time model data structure 🛛 🔲 Ci				
Configure Model Functions					
Data exchange					
MAT-file logging					
Interface: None					



Software-in-the-Loop Testing Embedded Coder

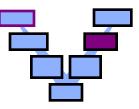


Test generation production code with your environment or plant model to verify a successful conversion of the model to code.

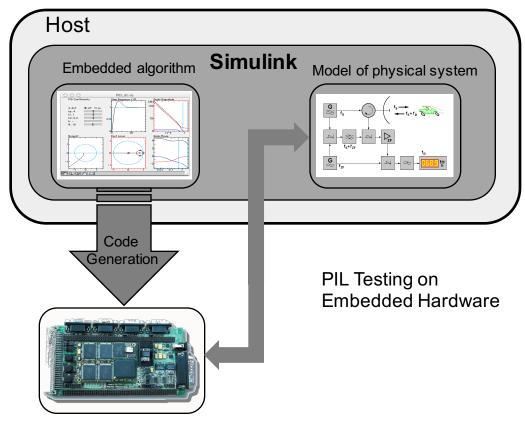




Processor-in-the-Loop Testing Embedded Coder



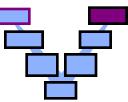
Use processor-in-the-loop PIL to evaluate the behavior of a candidate algorithm on the target processor.



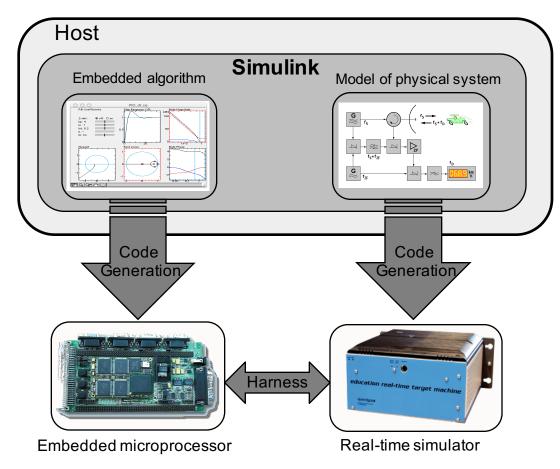
Embedded microprocessor



Hardware-in-the-Loop Testing Embedded Coder and Simulink Coder with Simulink Real-time

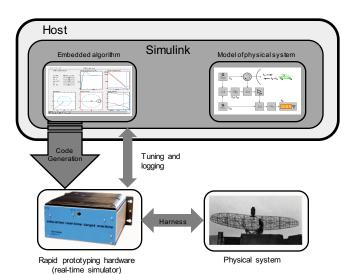


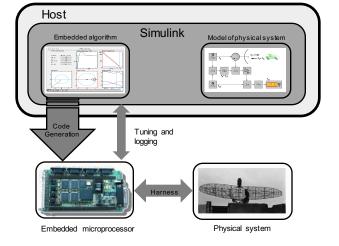
Final test before integration using simulated plant executing in real time.



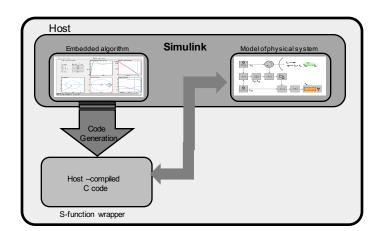


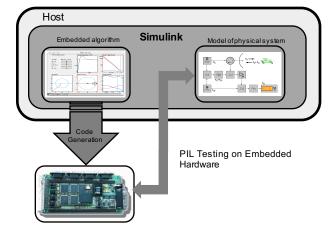
Usage of Code Generation Products

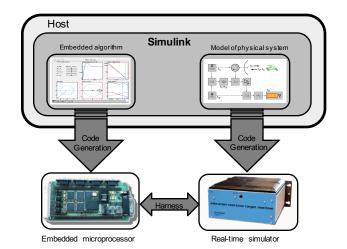




Þ 🧇 🎯 Find:	😚 🐓 Match Case		
Contents	Traceable Simulink Blocks	/ Stateflow Objects / MATLAB Functions	
Summary	Root system: iir_ert		
Subsystem Report	Object Name	Code Location	
Code Interface Report			
Traceability Report	< <u><root>/u</root></u>	iir_ert.c:34	
Static Code Metrics Report	Subsystem: iir ert/DocBlock		
Code Replacements Report	Subsystem: <u>m_crty boeblock</u>		
	No traceable objects in this Sub	osystem.	
Generated Code			
[-] Main file	Subsystem: <u>iir_ert/IIR_filter</u>		
ert_main.c	Object Name	Code Location	
[-] Model files	< <u><\$2>/Sum</u>	iir_ert.c:31	
<u>iir_ert.c</u>	<s2>/Unit Delay</s2>	iir_ert.c:20, 35, 39	
<u>iir_ert.h</u>		iir_ert.h:35	
	<u><\$2>/a1</u>	iir_ert.c:32	
<u>iir_ert_private.h</u>	62.4.0	iir ert.c:33	
iir_ert_private.h iir_ert_types.h	<u><\$2>/b0</u>	m_ercc.sz	
<u>iir_ert_types.h</u>	Subsystem: <u>iir_ert/Model Info</u>		







Embedded microprocessor



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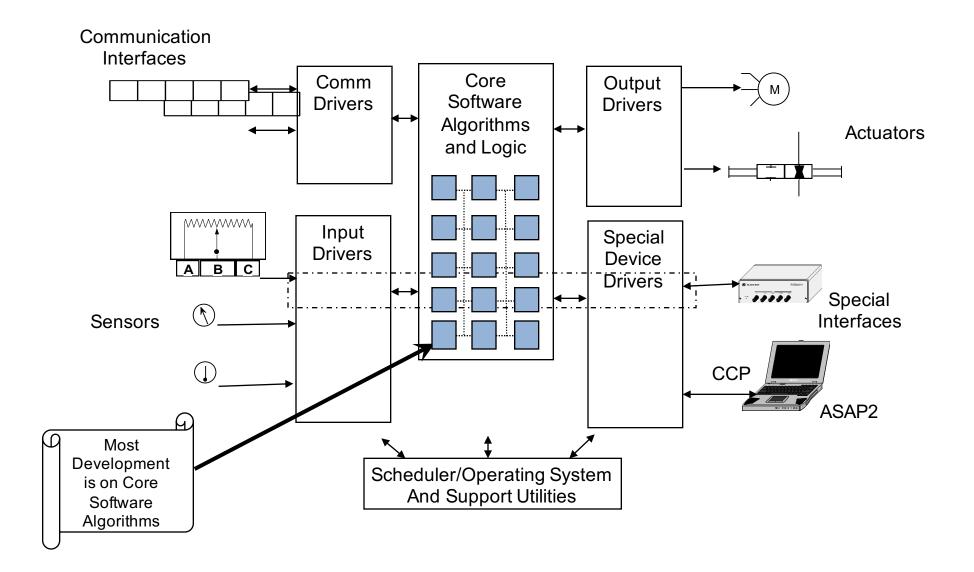


Example) Controller of Landing Gear

too 🔓	ntrol_system - Simulink
File	Edit View Display Diagram Simulation Analysis Code Tools Help
▶	• ', • , • , • , • , • , • , • , • , • ,
contr	rol_system
۲	Na control_system ►
Q	
5 7	
⇒	square Signal 1 double + double error ctrl_output double 3 DesiredOutput + - double error ctrl_output double 3 2.45e-4s ² +0.03s+0.2 PlantOutput + 1
ΕA	Signal Builder Out1
	PI_Algorithm Analog Plant
0	
>>	
Ready	y View diagnostics 100% ode4



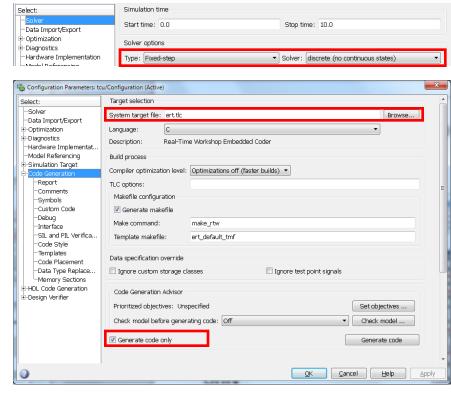
Simple Software Architecture

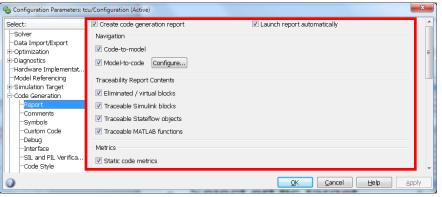




Basic Code Generation Workflow for Embedded Target

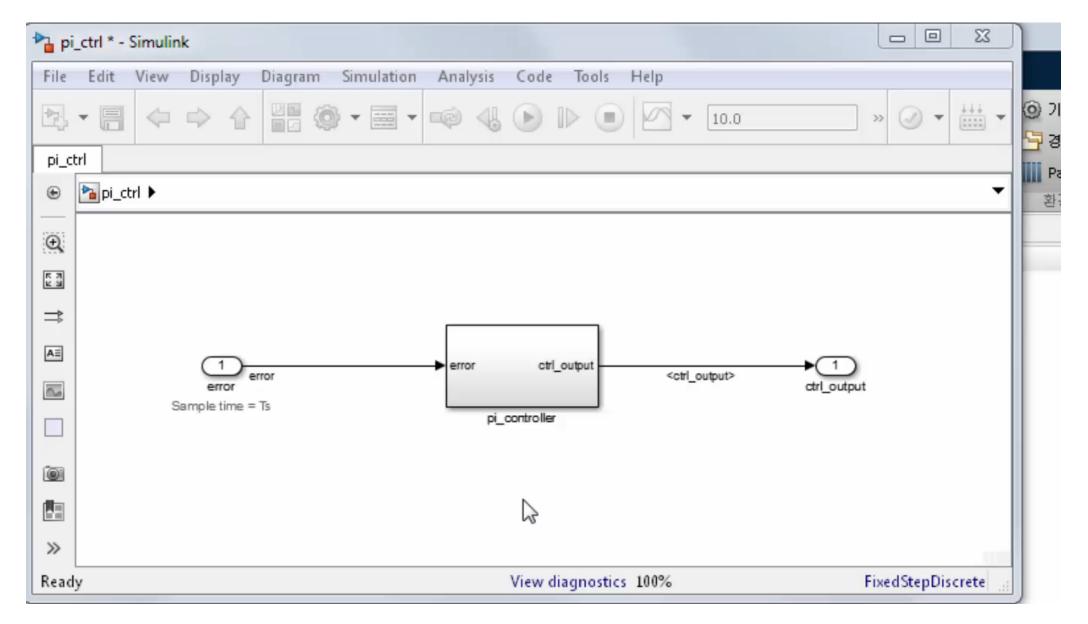
- Select solver to be fixed step with discrete
- Select ert.tlc target
- Select generate code only
- Select HTML Report for easy review
- Generate code for model
- Review code in browser







Demo: Code Generation Workflow





Code Generation Reports

- Subsystem Report
- Code Interface Report
- Traceability Report
- Static Code Metrics Report
- Code Replacements Report

Code Generation Report			
夺 🔿 🎯 Find:	分 🕹 Match Case		
Contents	Traceable Simulink Blocks / Sta	teflow Objects / MATLAB Functions	*
<u>Summary</u>	Root system: <u>iir_ert</u>		
<u>Subsystem Report</u> <u>Code Interface Report</u>	Object Name	Code Location	
Traceability Report	<u><root>/u</root></u>	iir_ert.c:34	
<u>Static Code Metrics Report</u> <u>Code Replacements Report</u>	Subsystem: <u>iir_ert/DocBlock</u>		
	No traceable objects in this Subsyster	n.	
Generated Code	Subautan in art/UD filter		
[-] Main file	Subsystem: <u>iir_ert/IIR_filter</u>		
<u>ert_main.c</u>	Object Name	Code Location	
[-] Model files	<u><\$2>/Sum</u>	iir_ert.c:31	
<u>iir_ert.c</u> <u>iir_ert.h</u>	< <u>S2>/Unit Delay</u>	iir_ert.c:20, 35, 39 iir_ert.h:35	
<u>iir_ert_private.h</u>	<u><\$2>/a1</u>	iir_ert.c:32	E
<u>iir_ert_types.h</u>	<u><\$2>/b0</u>	iir_ert.c:33	
[⁻] Utility files <u>rtwtypes.h</u>	Subsystem: <u>iir_ert/Model Info</u>		
	No traceable objects in this Subsyster	n.	-
			OK Help



Demo: Code Generation Reports

(Code Generation Report		
	< 🔿 🤄 Find:	삼 🦞 Match Case	
	Contents	Code Generatio	on Report for 'pi_ctrl'
	Summary	Summary	
	Subsystem Report	Summary	
	Code Interface Report	Code generation for model "pi	_ctrl"
	Traceability Report	Model version	1.10
	Static Code Metrics Report	Simulink Coder version	8.9 (R2015b) 13-Aug-2015
	Code Replacements Report	C source code generated on	Mon Feb 01 13:36:49 2016
		C source code generated at	C:\Applications\Seminars\PCG_Seminar\work\pi_ctrl_ert_rtw\
i_controller * - Simulink	Generated Code		c. / #preasons (services / co_services (non/(s)_con_cr(_r(c))
<u>V</u> iew <u>D</u> isplay Diag <u>r</u> am <u>Simulation</u> <u>A</u> nalysis <u>C</u> ode	[-] Main file	Configuration settings at the t	ime of code generation: click to open
	ert_main.c	Code generation objectives: U	nspecified
× pi_ctrl ×	[-] Model files	Validation result: Not run	
_ctrl > Pa pi_controller	pi_ctrl.c		8
	pi_ctrl.h		
	pi_ctrl_private.h		
	pi_ctrl_types.h		
error Sample time = Ts proportional_gain	[-] Utility files		
Sample time = is	rtwtypes.h		
		-	
sample_time_integral_gain			
View dia			OK Help

🔺 MathWorks

R2015b

Embedded Coder Quick Start

Easily configure Simulink Model to generate production code

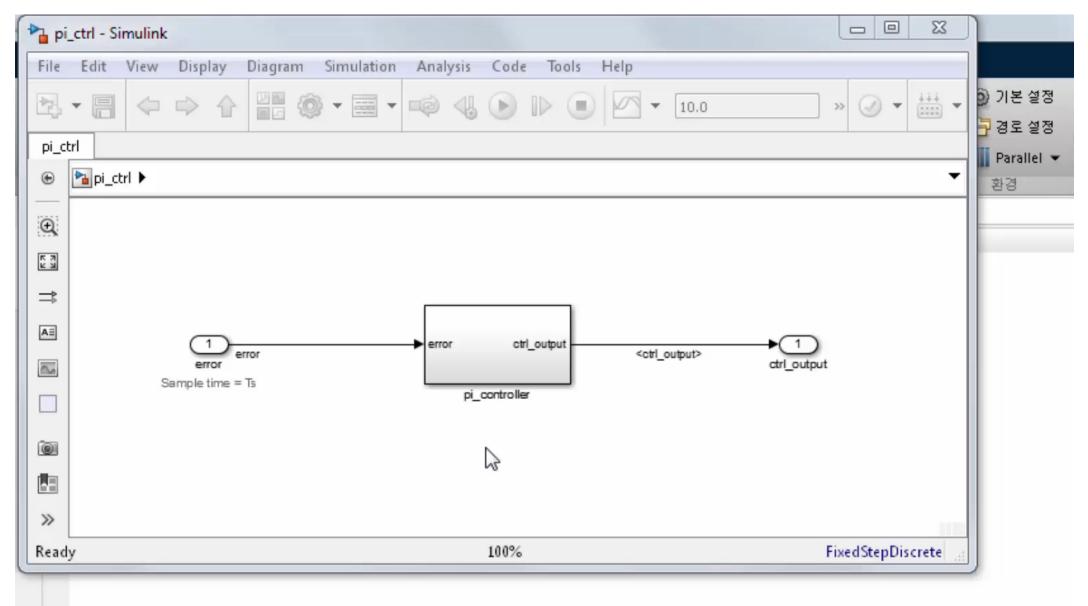
- Ask questions about code generation goals
- Auto configure and validate model against the selections
- Show recommended configuration changes
- Apply configuration changes and generate code

Code Tools Help		_		
C/C++ Code	•	8	Embedded Coder Quick Start	
HDL Code	•	$\mathcal{Q}_{\mathbf{a}}$	Code Generation Advisor	
PLC Code	ŀ		Code Generation Options	
Data Objects	•		Build Model	Ctrl+B

	ne > System > O	utput > Deployment > We	ord Size > Optimization	> Generate Code	
Rev	iew the recommended of	configuration parameter change	s for model: 'sldemo_fuelsy	s'. When you are ready to	apply the
chai	nges and generate code	e, click Next.			
Don	ding model configuratio	n paramotors changes:			
	0				
#	Category	Parameter	New Value	Old Value	
1	Code Generation	Prioritized objectives	Execution efficiency,RAM efficiency		
2	Code Generation	complex numbers	on	off	
3	Code Generation	continuous time	on	off	
4	Optimization	Optimize global data access	Minimize global data access	Use global to hold temporary results	
5	Optimization	Pack Boolean data into bitfields	off	on	
6	Optimization	Simplify array indexing	off	on	
7	Optimization	Use bitsets for storing Boolean data	off	on	
8	Optimization	Use bitsets for storing state configuration	off	on	



Demo: Embedded Coder Quick Start





Optimization Considerations

elect:	Simulation and code generation							
Solver Data Import/Export	Block reduction	🔽 Condi	tional input brand	ch execution				
 Optimization 	Implement logic signals as Boolean d Mapping Application Requirements to the Optimization Pane: General Tab							
Signals and Parameters Stateflow	Use division for fixed-point net slope co	Configuration Parameter	Settings for Buildi	ng Code			Factory Default	
 Diagnostics Hardware Implementation 	Use floating-point multiplication to ha		Debugging	Traceability	Efficiency	Safety precaution		
Model Referencing Simulation Target Code Generation	Default for underspecified data type:	Block reduction	Off (GRT) No impact (ERT)	Off	On	Off	On	
Report Comments	Code generation	Implement logic signals as Boolean data (vs. double)	No impact	No impact	On	On	On	
Symbols Custom Code Debug Interface Verification Code Style Templates Code Placement Data Type Replacement Memory Sections HDL Code Generation Optimize using Data initialization Remove root Integer and fixed Remove code Remove code Accelerating simul	 Optimize using the specified minimul Data initialization Remove root level I/O zero initialization 	Conditional input branch execution	No impact	On	On (execution) No impact (ROM, RAM)	No impact	On	
	🔲 Remove internal data zero initializa	Application lifespan (days)	No impact	No impact	Finite value	inf	inf	
	Integer and fixed-point Integer and fixed-point Remove code from floating-point to Remove code from floating-point to Remove code that protects against	Use memset to initialize floats and doubles to 0.0	No impact	No impact	On* (execution, ROM) No impact (RAM)	No impact	On	
	Accelerating simulations Compiler optimization level: Optimizat	Use floating-point multiplication to handle net slope corrections	No impact	No impact	On (when target hardware supports efficient multiplication) Off (otherwise)	Off	Off	
0		Remove code from floating-point to integer conversions that wraps out-of-range values	Off	Off	On (execution, ROM) No impact (RAM)	Off (GRT) On (ERT)	Off	
		Remove code from floating-point to integer conversions with wation that maps NaN	Off	Off	On			



Code Generation Objectives

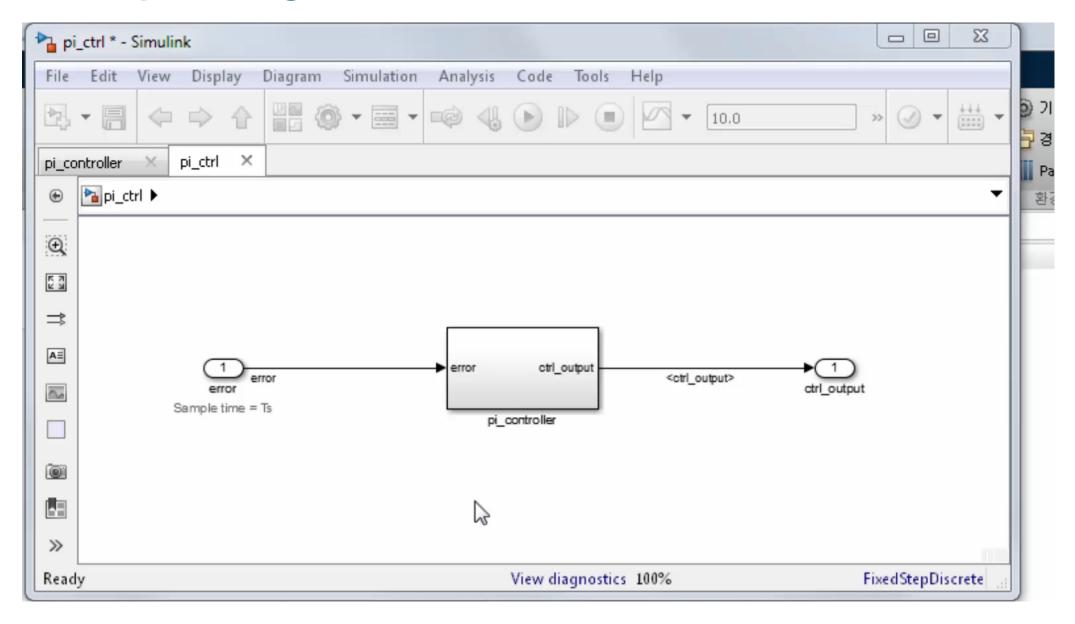
Configuration Parameters: pi_ctrl/C	onfiguration (Active)		
▷ Simulation Target	Build process		*
Code Generation	- Toolchain settings		
Report	-		
Comments Symbols	Toolchain:	Automatically locate an installed toolchain Validate	
Custom Code		Microsoft Visual C++ 2010 v10.0 nmake (64-bit Windows)	
Debug	Build configuration:	Faster Builds Show settings	
Interface Verification	-	Minimize compilation and linking time	
Code Style		Minimize compliadori and linking dine	Ξ
Templates Code Placement Data Type Replacement Memory Sections ▷ HDL Code Generation	Data specification ove	age classes I Ignore test point signals	
	Prioritized objectives		
	Check model before	generating code: Off Check Model	
	Generate code only	Generate Code	
	🔲 Package code and	artifacts Zip file name:	
			Ŧ
0		QK <u>Cancel</u> Help Apply	
×			

- Models have a lot of possible settings
- Code Generation Objectives gives a starting point

Description Gelect and prioritize your code generati	n objectives. You can add custom	
objectives, for details, see the documen		
Available objectives	Selected objectives - prioritized	
Execution efficiency ROM efficiency		
RAM efficiency Traceability		(
Safety precaution Debugging	+ I	(
MISRA-C:2004 guidelines Polyspace		



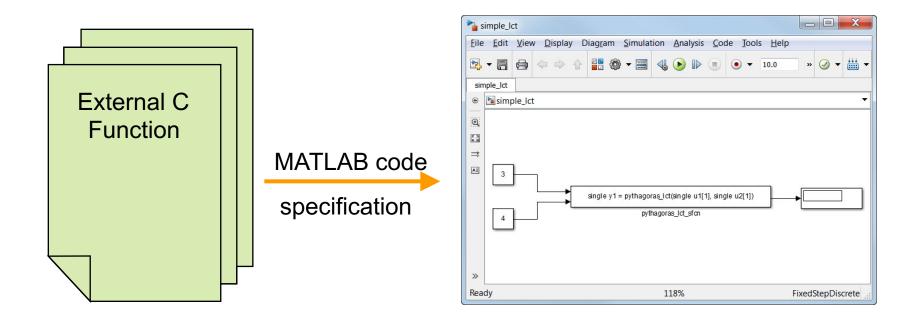
Demo: Optimizing Generated Code





Legacy Code Tool

- Legacy Code Tool is a utility that generates an S-function automatically from existing C code
- It can also insert an appropriate call to generated code





Demo: Code Generation with Legacy C Code

☑ 편집기 - C:\Applications\Seminars\PCG_Seminar\src\pi_ctrl_legacy.c	
편집기 보기 🔂 Seminars 🚵 Work 🛃 🔚 🔬 🛅 😒 😅 🔂 🕐 💿	x
····································	1
pi_ctrl_legacy.c x pi_ctrl_legacy.h x pi_ctrl_lct.m x +	
1 2 #nclude "pi_ctrl_legacy.h" 3 4 real_T yi_prev;	
5	
6 real_T pi_control(real_T error) 7 {	
8 real_T temp_yi;	
9 real_T ctrl_output;	
10 11 /* Calculate yi */	
12 temp_yi = 0.01 * error * 2.0 + yi_prev;	
13 14 /* pi_control output */	
15 ctrl_output = 0.3 * error + temp_yi;	
16 17 /* yi state update */	
18 yi_prev = temp_yi;	
19 20 return ctrl_output;	
21 }	
22 23	



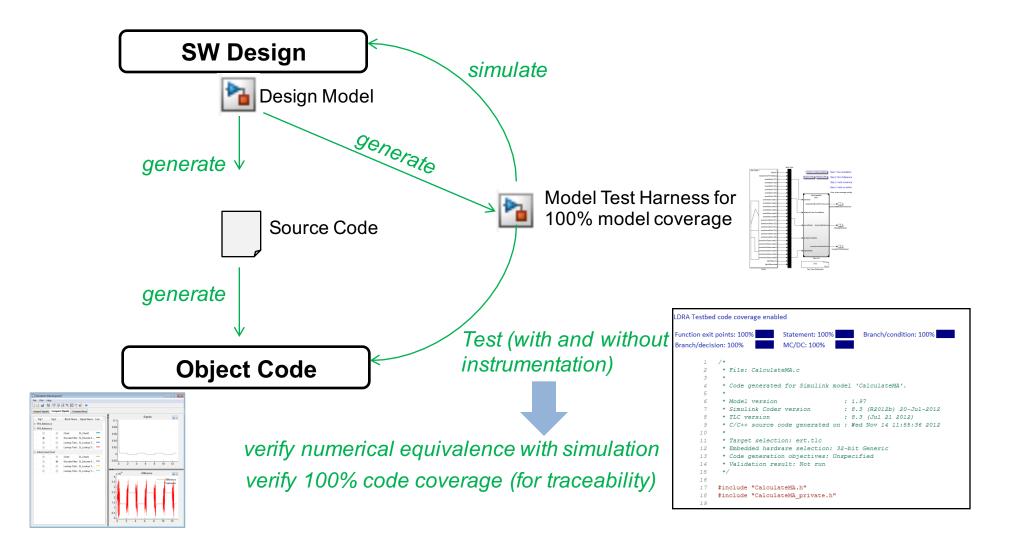
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Equivalence Test

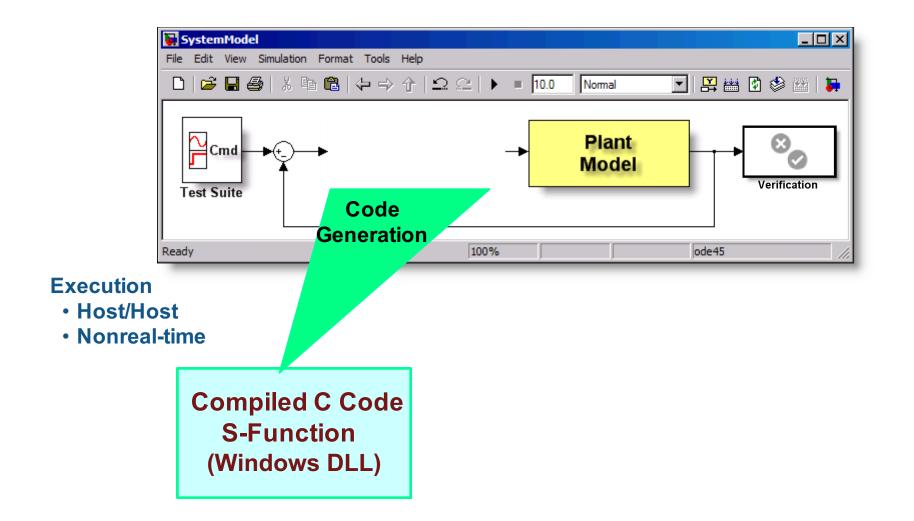
SIL (Software-In-the-Loop) and PIL (Processor-In-the-Loop)





Software-in-the-Loop (SIL) Testing:

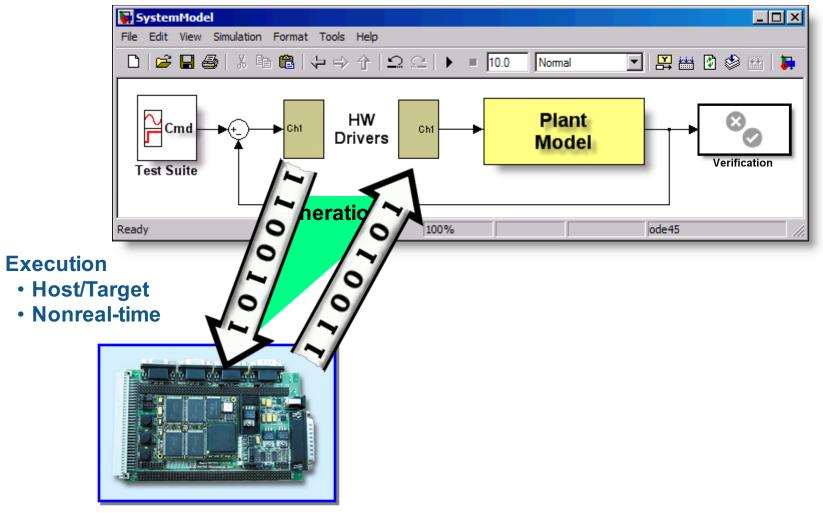
Verify Production Controller with Software-in-the-loop





Processor-in-the-Loop Testing:

Verify Production Controller with Processor-in-the-loop





Processor-in-the-Loop (PIL) API

Problem

- Embedded IDE Link does not support PIL for an arbitrary combination of
 - Processor
 - Compiler
 - Debugger or download utility
 - Communications channel

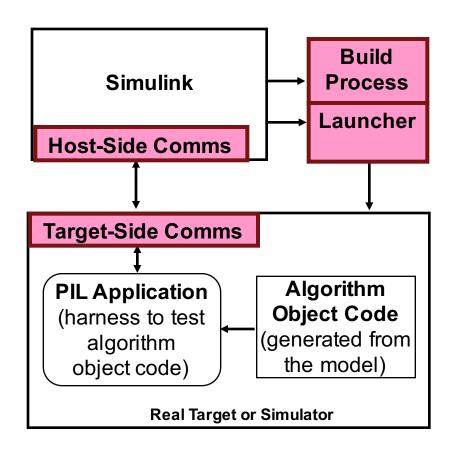
Solution

- Provide an API that allows integration of third-party or customer tools for
 - Building the PIL application
 - Downloading and running the application
 - Communicating with the application

Benefit

- The power of PIL verification is easily adaptable for any target environment
- A fully documented API is stable across MathWorks releases

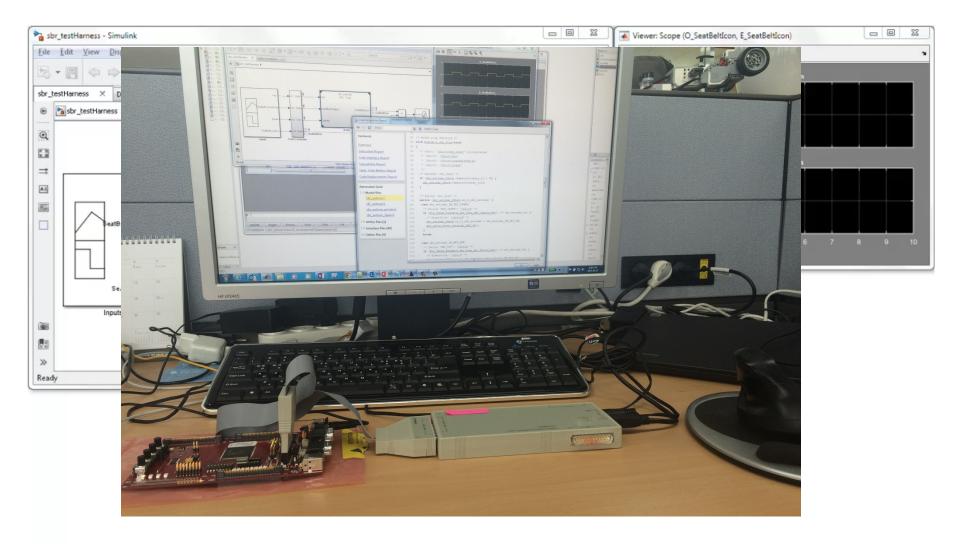
PIL API Components





PIL Testing Example

Infineon Tricore with Trace32 Debugger





Key Benefits of SIL and PIL

- Reuse test vectors for simulation, SIL and PIL
 - Verify correct execution behaviour of compiled code (including on production hardware)
 - Collect metrics for the generated code
 - Code coverage
 - Execution profiling
 - Stack profiling
- Evaluate hardware specific optimizations
- Generate artifacts for IEC-61508, IEC-62304, ISO-26262, EN-50128, and DO-178 certification
- Early verification and fixing of defects reduces cost

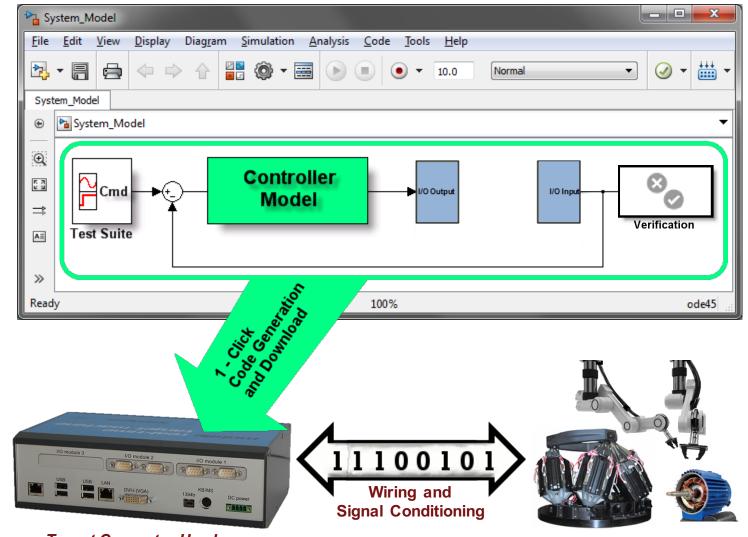


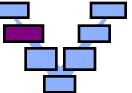
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Real-Time Simulation and Testing Tasks: Rapid Controls Prototyping





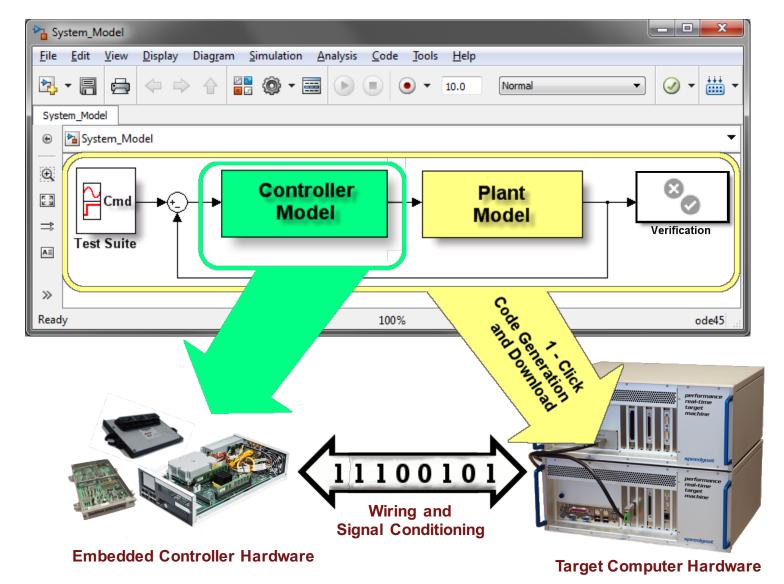
Physical Plant Hardware

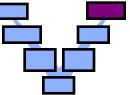
Target Computer Hardware



Real-Time Simulation and Testing Tasks:

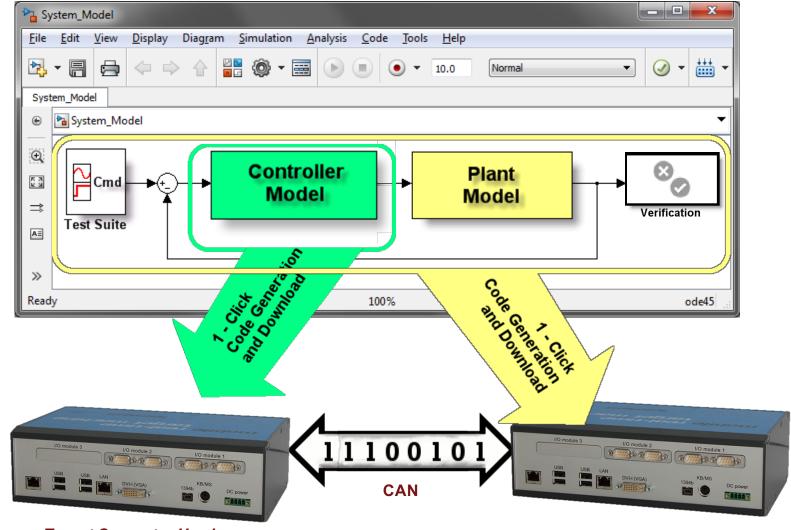
Hardware-in-the-loop (HIL) Simulation







Today's Configuration



Target Computer Hardware



What is Simulink Real-Time?

From desktop simulation to real time



Creation of real-time applications from Simulink models and loading them onto dedicated target computer hardware in 3 automated steps:





What is Simulink Real-Time?

Connect to your physical system

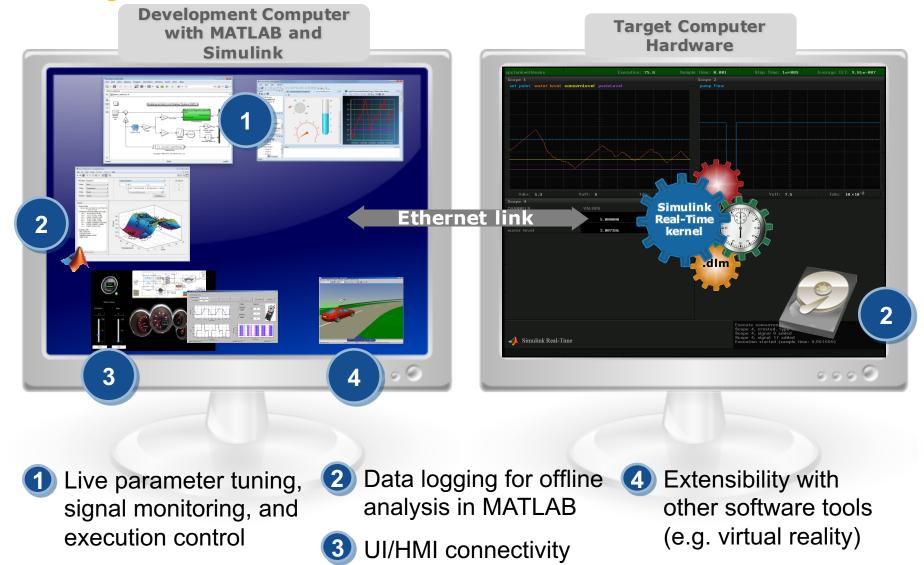


- Support for a broad range of I/O types and communication protocols
- Easy drag and drop and configuration within a Simulink model



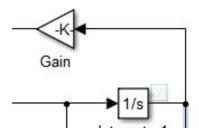
What is Simulink Real-Time?

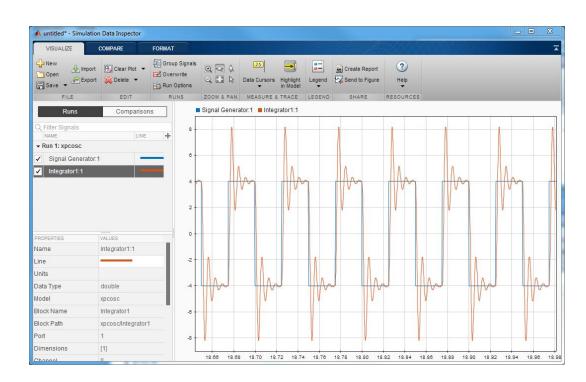
Extendable, integrated, and interactive





Streaming to the Simulation Data Inspector





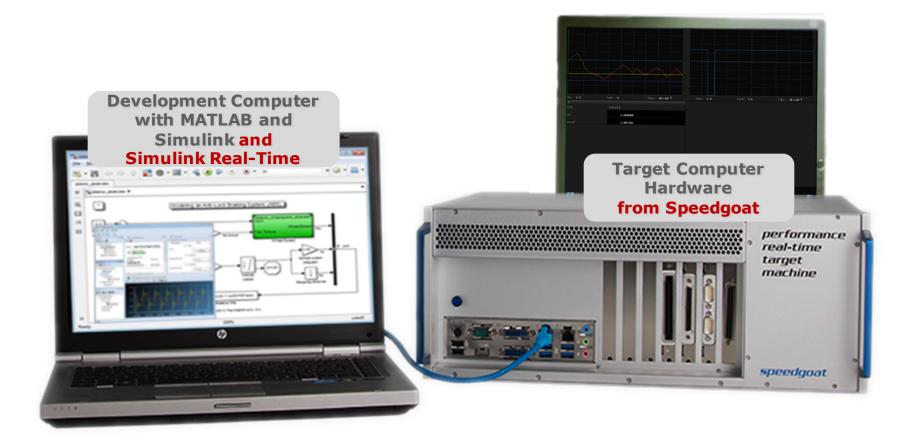
- 1. Select the signals to stream
- 2. Connect to the running target computer
- 3. Visualize in the Simulation Data Inspector





What Hardware is used with Simulink Real-Time?

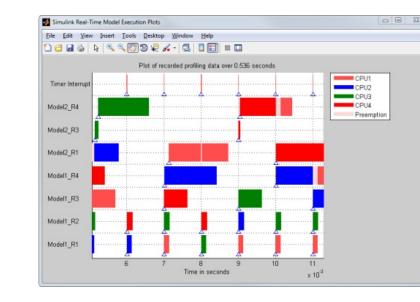
Development computer + target computer



42



Current Performance Level

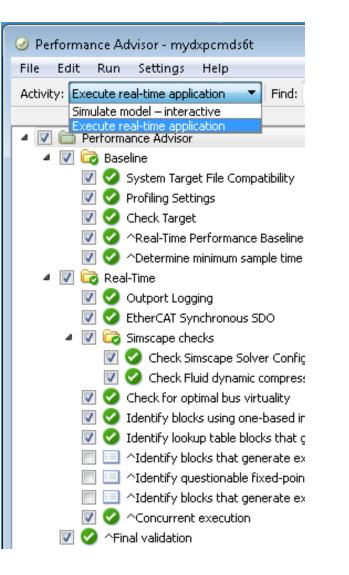


real-time multi-core scheduler

- 25 microsecond minimum sample time
- < 1 microsecond sample time with FPGA's
- High performance quad core Intel processors
- Expandable, low latency I/O

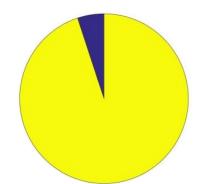


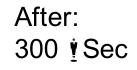
Performance Advisor for Real-Time Execution

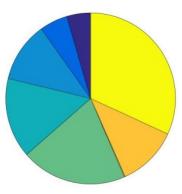


- Encodes best practices for transitioning to real-time
- Adds testing on the target computer.

Before: 4000 <u>¥</u>Sec





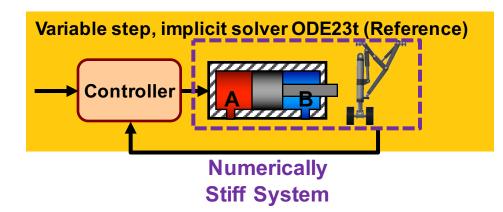






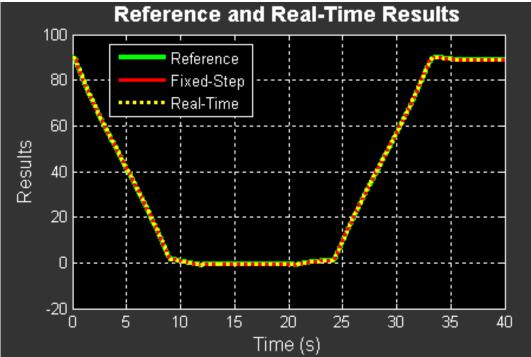
Configuring Landing Gear Model for HIL Testing

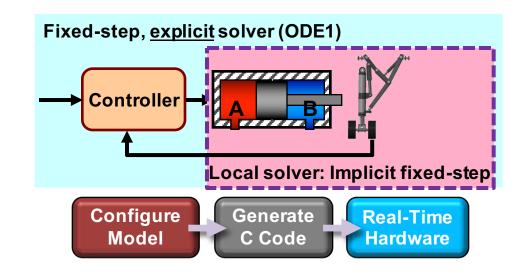
Model:



Problem: Configure solvers to minimize computations so the model can simulate in real time

Solution: Use local solvers on stiff physical networks and explicit solvers elsewhere







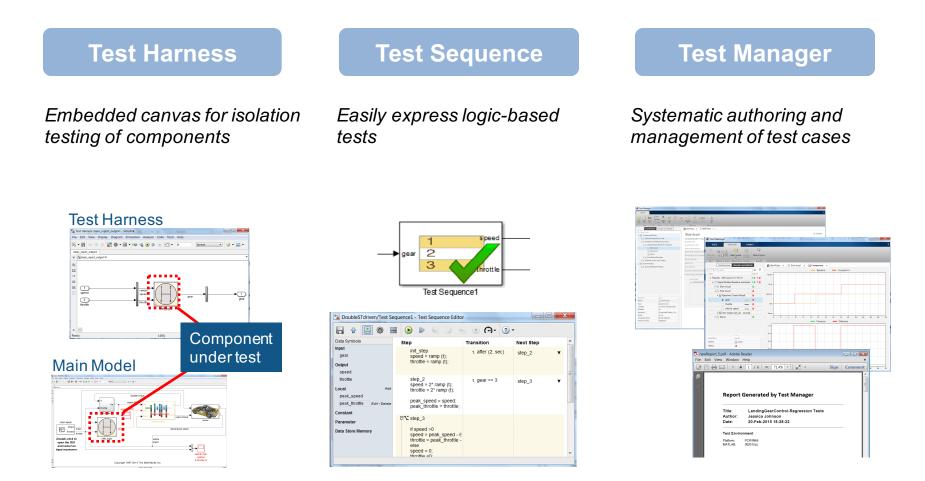
Agenda

- Production Code Generation
 - MathWorks' Code Generation Products
 - Embedded Coder
 - Equivalence Test with SIL and PIL
- Integration Test
 - What's Simulink Real-Time
 - Automation of Real-Time Testing



Let's remind Simulink Test....

Tool for authoring, managing, and executing simulation-based tests





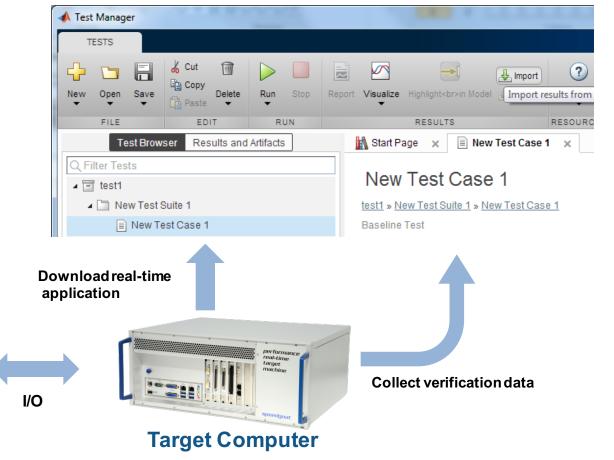
Test Automation with Simulink Test

- Available to verify algorithm in real-time
 - Reusing Test Harness and Test Sequence in Simulink Test
 - Avoiding multiple build/download to target
 - Avoiding additional programing to access test results

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Controller

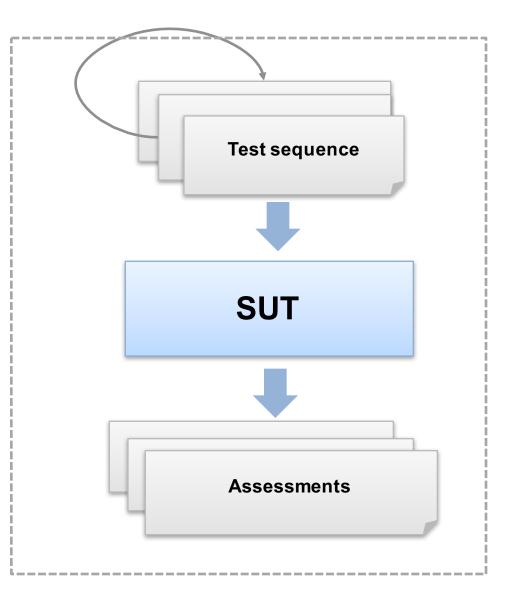
Physical System





Key Design Principles

- Use Test Sequence Block for Assessments
 - Evaluated in real-time on target
 - Non-fatal verification language
 - Failure does not stop execution
 - Language constructs for fault recovery
 - Prevent hardware damage
- Runtime variants
 - Avoid multiple build/download to target
- Rapid Iterations
 - Over runtime variants on target hardware





Summary

- Production Code Generation
 - You can get a code for production without human error.
 - Embedded Coder provides "Quick Start" for beginner to try code generation easily.
- Real-Time Testing
 - You can get many benefits with real-time testing
 - Reduce hardware testing
 - Avoid breaking expensive equipment
 - Improve product quality
 - You can do real-time testing in one environment with Simulink.
 - For real-time testing, you can reuse all test cases developed to verify models.